AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-4. (Cancelled)

5. (Previously Presented) A semiconductor chip comprising:

a semiconductor substrate;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode which is formed in a through-hole of the semiconductor substrate from a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate, and a second insulating section that covers a remaining region of the second surface of the semiconductor substrate, the first insulating section being connected to the second insulating section by a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section;

wherein the second insulating section is formed to be thinner than a thickest area of the first insulating section.

6. (Original) The semiconductor chip as defined in claim 5, wherein the first insulating section is formed so that a thickness of the first insulating section decreases as a distance from the projection increases.

7. (Original) The semiconductor chip as defined in claim 5, wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

8. (Original) The semiconductor chip as defined in claim 5, wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

9-18. (Cancelled)

19. (Previously Presented) A semiconductor wafer comprising:

a semiconductor substrate;

a plurality of integrated circuits, at least a part of each of the integrated circuits being formed in the semiconductor substrate;

a plurality of penetrating electrodes, each of the penetrating electrodes being formed in through-holes of the semiconductor substrate from a first surface to a second

surface of the semiconductor substrate, the through-holes having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrodes each having a projection which projects from the second surface; and

an insulating layer formed over an entire surface of the second surface of the substrate, the insulating layer including a plurality of first insulating sections and a second insulating section other than the first insulating sections, each of the first insulating sections being formed in regions that surround the projections above the second surface of the substrate such that the projections define through-bores in the first insulating sections, and the second insulating section covering a remaining region of the second surface of the semiconductor substrate, the first insulating sections being connected to the second insulating section by radially tapering arcuate portions having a varying radius of curvature from the through-bore to the second insulating section;

wherein the second insulating section is formed to be thinner than a thickest area of each of the first insulating sections.

20. (Original) The semiconductor wafer as defined in claim 19, wherein each of the first insulating sections is formed so that a thickness of each of the first insulating sections decreases as a distance from the projection increases.

21. (Original) The semiconductor wafer as defined in claim 19, wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

22. (Original) The semiconductor wafer as defined in claim 19, wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

23-33. (Cancelled)

34. (Original) A circuit board on which the semiconductor chip as defined in claim 5 is mounted.

35-41. (Cancelled)

42. (Original) An electronic instrument comprising the semiconductor chip as defined in claim 5.

43-70. (Cancelled)